Control Inputs

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Operation | opcode | func | Reg select to write data | Reg wrt | Imm load | A invert | B invert | ALU op | Store enbl | Load enbl | Mem slct | beq | Jump slct | DISP  Cntrl |
| ADD | 000 | 0 | 01 | 1 | 00 | 0 | 0 | 11 | 0 | 0 | 00 | 0 | 0 | 0 |
| SUB | 000 | 1 | 01 | 1 | 00 | 0 | 1 | 11 | 0 | 0 | 00 | 0 | 0 | 0 |
| ADDi | 001 | \* | 00 | 1 | 01 | 0 | 0 | 11 | 0 | 0 | 00 | 0 | 0 | 0 |
| LW | 010 | \* | 10 | 1 | 01 | 0 | 0 | 11 | 0 | 1 | 01 | 0 | 0 | 0 |
| SW | 011 | \* | 10 | 0 | 01 | 0 | 0 | 11 | 1 | 0 | 01 | 0 | 0 | 0 |
| BEQ | 100 | \* | 00 | 0 | 10 | 0 | 1 | 11 | 0 | 0 | 00 | 1 | 0 | 0 |
| SLTI | 101 | \* | 10 | 1 | 01 | 0 | 1 | 11 | 0 | 0 | 10 | 0 | 0 | 0 |
| J | 110 | \* | \*\* | 0 | \*\* | \*\* | \*\* | \*\* | 0 | 0 | \*\* | 0 | 1 | 0 |
| DISP | 111 | \* | \*\* | 0 | \*\* | \*\* | \*\* | \*\* | 0 | 0 | 11 | 0 | 0 | 1 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |